IN THE CLAIMS

Please amend the claims as follows:

1. An integrated circuit comprising:

a test circuit configured to generate a test signal having a predetermined pulse width in response to a control input, wherein said test signal tracks process corners and can be used to predict a failure of said integrated circuit.

2. The integrated circuit according to claim 1, wherein said control input comprises a write enable input.

3. The integrated circuit according to claim 2, wherein said control input comprises a transition of a write enable input.

4. The integrated circuit according to claim 3, wherein said transition is from a HIGH logic level to a LOW logic level.

5. The integrated circuit according to claim 1, wherein said pulse width is user definable.

6. The integrated circuit according to claim 5, wherein said pulse width is determined in response to one or more configuration inputs.

7. The integrated circuit according to claim 6, wherein said configuration inputs are fuse programmable.

8. The integrated circuit according to claim 6, wherein said configuration inputs are determined by a metal masking step during fabrication.

9. The integrated circuit according to claim 1, wherein said integrated circuit comprises a static random access memory.

10. The integrated circuit according to claim 9, wherein said test circuit is configured to predict a failure of one or more memory cells.

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11. (AMENDED) An integrated circuit comprising:

means for generating a test signal having a predetermined pulse width in response to a control input; and

means for predicting failure of part or all of said integrated circuit in response to said test signal.

12. (AMENDED) A method for predicting failure of an integrated circuit prior to life testing comprising the steps of:

(A) entering a test mode;

(B) measuring an operation of said integrated circuit in response to a test signal having a predetermined pulse width and generated on said integrated circuit in response to a control input; and

(C) detecting failure of said operation.

13. The method according to claim 12, wherein said operation comprises a write operation.

14. The method according to claim 12, wherein said test signal is a write pulse.

15. The method according to claim 14, wherein said write pulse has a pulse width determined by a data setup to write end time of the integrated circuit.

16. The method according to claim 12, wherein the steps (A)-(C) are performed prior to life testing.

17. The method according to claim 12, further comprising the step of:

(D) sorting said integrated circuits in response to said failure.

18. The method according to claim 17, further comprising the step of:

(E) repairing said integrated circuit.

19. The method according to claim 12, wherein said failure comprises a poor contact in cross-coupled latch transistors of a memory cell.

20. The method according to claim 12, wherein step (A) comprises the sub-steps of:

(A-1) applying a first high voltage to an address pin of said integrated circuit;

(A-2) applying a second high voltage to an enable pin of said integrated circuit; and

(A-3) removing said first high voltage from said address pin.

Please add the following new claims:

21. (NEW) The integrated circuit according to claim 1, wherein said test circuit is further configured (i) to generate said test signal having said predetermined pulse width when in a first mode and (ii) to pass said control input as said test signal when in a second mode.

22. (NEW) The integrated circuit according to claim 21, wherein said test circuit is further configured to enter said first mode in response to a predetermined sequence of input signals.

23. (NEW) The integrated circuit according to claim 1, wherein said test circuit comprises:

a first circuit configured to generate said test signal in response to said control input and a control signal; and

a second circuit configured to generate said control signal in response to a plurality of input signals.